less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process temperature of from about 300 to 500°C; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

Remarks

Examiner Brewster is thanked for the thorough Office Action.

In the Claims

Independent claims 32 to 34 are new and have been added to better encompass the full scope and breadth of the invention notwithstanding the patentability of the original claims. Claims 32 to 34 correspond to independent claims 1, 11 and 20, respectively and include a 'whereby' clause at their ends thereof.

Claim Rejections

The Rejection Of Claims 1, 2, 8 To 11, 17 To 20 And 26 To 31 Under 35 U.S.C. §103(a) as Being Unpatentable Over Perng et al. (U.S. Patent No. 6,149,987) In View Of Ngo (U.S. Patent No. 6,054,735)

The rejection of claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 under 35 U.S.C. §103(a) as being unpatentable over Perng et al. (U.S. Patent No. 6,149,987) (the '987 Perng Patent) in view of Ngo (U.S. Patent No. 6,054,735) (the '735 Ngo Patent) is acknowledged.

The Rejection Of Claims 3 To 7, 12 To 16 And 21 To 25 Under 35 U.S.C. §103(a) as Being Unpatentable Over Perng et al. (U.S. Patent No. 6,149,987) In View Of Ngo (U.S. Patent No. 6,054,735) As Applied To Claims1, 2, 8 To 11, 17 To 20 And 26 To 31, And Further In View Of Tao (U.S. Patent No. 5,904,566)

The rejection of claims 3 to 7, 12 to 16 and 21 to 25 under 35 U.S.C. §103(a) as being unpatentable over Perng et al. (U.S. Patent No. 6,149,987) (the '987 Perng Patent) in view of Ngo (U.S. Patent No. 6,054,735) (the '735 Ngo Patent) as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 above and further in view of Tao (U.S. Patent No. 5,904,566) (the '566 Tao Patent) is acknowledged.

Applicants' wish to briefly point up the claimed features of their invention which are believed to be not shown nor obvious from the teachings of known references in this field. The claims all clearly define:

(1) pre-coating the inner walls of a CVD chamber with a first PECVD silicon oxide film having a first thermal CVD oxide deposition rate;

(2) placing a semiconductor wafer within the pre-coated CVD chamber, the wafer having an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate that is less than the first thermal CVD oxide deposition rate of the first PECVD silicon oxide film coating the inner walls of the CVD chamber; and

(3) depositing a porous silicon oxide film upon the semiconductor wafer's second PECVD silicon oxide film, the porous silicon oxide film being different from the first PECVD silicon oxide film coating the inner walls of the CVD chamber and such that the porous silicon oxide film is deposited upon the PECVD silicon oxide film coating the inner walls of the CVD chamber at a faster rate than upon the semiconductor wafer's second PECVD silicon oxide film.

The '735 Ngo Patent teaches away from the claimed instant invention as it discloses seasoning a chamber with a film material and then depositing the *same* film material on a wafer.

The '987 Perng Patent not only does not disclose a pre-coating step, for which the Examiner cites Ngo, the combination does not disclose or teach that the

(1) second thermal CVD oxide deposition rate (referring to the subsequently formed porous silicon oxide film) upon the upper second PECVD silicon oxide film on the semiconductor wafer is less than the

(2) first thermal CVD oxide deposition rate (referring to the subsequently formed porous silicon oxide film) upon the first PECVD silicon oxide film on the CVD chamber walls.

To further differentiate over the cited combination, the porous silicon oxide film 20 deposited upon the semiconductor wafer's 18 second PECVD silicon oxide film 22 is different from the first PECVD silicon oxide film 16 pre-coated upon the inner walls 14 of the CVD chamber 10.

Thus, independent claims 1, 11, 20, 32, 33 and 34 distinguish over: (1) the '987 Perng Patent in view of the '735 Ngo Patent under §103(a); and (2) the '987 Perng Patent in view of the '735 Ngo Patent as applied to claims 1, 2, 8 to 11, 17 to 20 and 26 to 31 above and further in view of the '566 Tao Patent under §103(a); for the above reasoning and further because the prior art lack a suggestion that the reference should be modified in a manner required to meet the claims; the invention is contrary to the teaching of the Ngo Patent—that is, the invention goes against the grain of what the prior art teaches; the Examiner has made a strained interpretation of the references that could be mode only be hindsight; the Examiner has not presented a convincing line of reasoning as to why the claimed subject matter as a whole, including its differences over the prior art, would have been obvious; and the prior art references do not contain any suggestions (express or

implied) that they be combined, or that they be combined in the manner suggested; the references take different approaches.

Claims 2 to 10 and 29 depend from independent claim 1; claims 12 to 19 and 30 depend from independent claim 11; claims 21 to 28 and 31 depend from independent claim 20; and are believed to distinguish over the combination for the reasons previously cited.

Therefore claims 1 to 34 are submitted to be allowable over the cited references and reconsideration and allowance are respectfully solicited.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectively requested. Allowance of all claims is requested. Issuance of the application is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

It is requested that the Examiner telephone Stephen G. Stanton, Esq. (#35,690) at (610) 296 – 5194 or the undersigned attorney/George Saile, Esq. (#19,572) at (845) 452 – 5863 if the Examiner has any questions or issues that may be

resolved to expedite prosecution and place this Application in condition for Allowance.

Respectively submitted,

Stephen B. Ackerman

Reg. No. 37,761

Version with markings to show changes made.

Please add the following new independent claims:

-- 32. A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

33. A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film.

34. A method for forming porous silicon oxide film, comprising the steps of:

providing a CVD chamber having inner walls and a wafer chuck/heater;

pre-coating at least a portion of the CVD chamber inner walls with a layer of first PECVD silicon oxide film having a first thermal CVD oxide deposition rate thereupon;

placing a semiconductor wafer on the wafer chuck/heater within pre-coated CVD chamber; the semiconductor wafer including an upper second PECVD silicon oxide film having a second thermal CVD oxide deposition rate thereupon that is

less than the first thermal CVD oxide deposition rate upon the first PECVD silicon oxide film coating the CVD chamber inner walls;

pre-heating the semiconductor wafer; and

depositing a porous silicon oxide film upon the upper second PECVD silicon oxide film overlying the semiconductor wafer by a thermal CVD process temperature of from about 300 to 500°C; the porous silicon oxide film being different from the first PECVD silicon oxide film coating the CVD chamber inner walls; whereby the porous silicon oxide film deposits faster upon the first PECVD silicon oxide film than on the upper second PECVD silicon oxide film. --